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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,367	09/04/2003	Michael Norman Day	AUS920020474US1	8438

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EXAMINER	
DOAN, DUC T	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/655,367	DAY ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-42* is/are rejected.

7)☒ Claim(s) *28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/31/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-21 have been presented for examination in this application. In response to the last Office Action, specification is amended, claims 1-21 were cancelled, claims 22-42 were added. As a result, claims 22-42 are now pending in the application.

Applicant's arguments filed 1/23/06 have been fully considered but they are mooted in view of new ground(s) of rejection necessitated by the Applicant's amendments to the claims.

All rejections and objections not explicitly repeated below are withdrawn.

Claim Rejection 35 USC 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 38 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 38 recites " a computer program product ...having a medium with a computer program embodied thereon..". There is no requirement in the claim for storing the program in a computer readable medium that executed by a computer. Without the combination with a stored medium, the computer program product with the computer program is a descriptive material and is not statutory because it is not capable of casing functional change in the computer.

All dependent claims are rejected as having the same deficiencies as the claims they depend from.

Claim Objections

Claim 28 are objected to because of the following informalities:

The claim's recitation "the a set of the L2" should be changed to "the set of the L2"

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 22-23,25-26,29-30,32-36,38,40-42 rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al (US 6425058) in view of Arimilli et al (US 6430656).

As for claim 22, Ar'058 describes a system for managing cache replacement eligibility, comprising: a first address register configured to request an address from an L1 cache (Ar'058 column 4 lines 1-30 describes registers that contains addresses for fetching instructions and fetching and storing operand in L1 caches, Fig1);

the claim further recites an L1 cache configured to determine whether a requested address is in the L1 cache and, in response to a determination that a requested address is not in the L1 cache, further configured to transmit the requested address to a range register coupled to the L1 cache; Ar'058 does not describe the claim's detail of address range register. However, Ar'656 describes a cache in which congruence classes are grouped into partitions of the cache (Ar'656 column 5 lines 50-65). Ar'656 Fig 2, column 6 line 58 to column 7 line 25 further describes the group selector and congruence class selector using address range comparison to produce address indexing into the cache. Thus an address range register must be used to compare with the incoming address and to generate the address indexing to cache via the group selector and congruence class selector circuits. It would have been obvious to one of ordinary skill in the art at the time of invention to include the congruency class cache and address indexing techniques as suggested by Ar'656 in Ar'058's system to map address ranges in cache based on the concurrency group information thereby using the cache more effectively for applications running in multiple processors system (Ar'656 column 4 lines 45-68);

the claim further recites the range register configured to generate a class identifier in response to a received requested address and to transmit the requested address and class identifier to a replacement management table coupled to the range register; the replacement management table configured to generate L2 tag replacement control indicia in response to a received requested address and class identifier; (Ar'656 column 6 line 57-67, the congruence classes information "class identifier" in address field 16 is used in the directory Fig 2: #20, information in the directory are used to generate group selector and congruence class selector that determine which cache location to be replaced, Ar'656 column6 lines 1-46).

an L2 address register coupled to the first address register and configured to request an address from an L2 cache; an L2 cache coupled to the L2 address register and the replacement management table and configured to determine whether a requested address is in the L2 cache and further configured to assign replacement eligibility of at least one set of cache lines in the L2 cache in response to received L2 tag replacement control indicia, (Ar'656 clearly describes the congruence classes are mapped into certain associate sets of the cache, column 6 lines 1-46).

and in response to a determination that a requested address is not in the L2 cache, the L2 cache further configured to overwrite a cache line within a set of the 1,2 cache ms a function of the replacement eligibility. Ar'656 clearly describes the congruence classes are mapped into certain associate sets of the cache, and allowing the replacement of cache entries in column 6 lines 24-36,

As in claim 23, the claim recites wherein a set of the L2 cache is replaced as a function of the replacement eligibility and a least recently used function (Ar'656 column 6 lines, selectively placing congruence classes data into certain sets of the cache, and replacement data among these assigned sets, Ar'656 lines 50-65).

As in claim 25, the claim recites wherein the range register and the replacement management table are further configured to be written to by software (Ar'656 column 7 lines 7-15).

As in claim 26 the claim recites wherein the range register comprises a range start register and a range mask register. Ar'656 column 7 lines 15-30 describes the group selector is capable of compare address ranges of cache regions with flexible block sizes. To accommodate the variable blocks size that impact the size of the region, it has been known in the art to provide

address masking register that masks out the least significant bits in the starting address received, thus providing the function of matching flexible address ranges or sizes.

Claims 29-30,38,41-42 rejected based on the same rationale as in the rejection of claim 22.

Claims 32,40 rejected based on the same rationale as in the rejection of claim 23.

Claims 33,36 rejected based on the same rationale as in the rejection of claim 24.

As in claim 34, the claim recites wherein the steps of setting a class identifier to a default value and setting a class identifier to a predetermined value further comprise employing a range register. Arimilli'656 column 6 lines 33-45 teaches that certain blocks' physical addresses can be absent from memory mapping and they are categorized as unused pages, Arimilli'656 column 5 line 50 to column 6 line 5 further teaches a technique for the block addresses received that in exceeding of the mapping to the associative numbers, these blocks should be mapped to the partition with the same property of unused associative bit. Thus Arimilli'656 clearly suggests of mapping these blocks into a default category/class of unused pages for caching purpose.

Claim 35 rejected based on the same rationale as in the rejection of claim 26.

Claims 24,37 rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al (US 6425058), Arimilli et al (US 6430656) as applied to claims 22,29 respectively and further in view of Arimilli et al (US 5974507).

As in claim 24, the claim recite wherein the L1 cache is one of the group comprising an L1 data cache and an L1 instruction cache. Ar'058 does not describe the claim's split L1 cache. However, Ar'507 describes a congruence cache that is capable to dynamically partitioning its

storage to accommodate for split I/D caching (Ar'507 column 3 lines 10-25). It would have been obvious to one of ordinary skill in the art at the time of invention to include the partitioning method as suggested by Ar'507 in Ar'058's system thereby using the cache more effectively by optimizing the cache partitioning accordingly by software applications characteristic running on the system (Ar'507 column 3 lines 15-25);

Claim 37 rejected based on the same rationale as in the rejection of claim 24.

Claims 27-28,31,39 rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al (US 6425058), Arimilli et al (US 6430656) as applied to claims 22,29 respectively and further in view of Arimilli et al (US 5974507) and McClure (US 5708789).

As in claim 27, the claim recites wherein the replacement management table comprises a plurality of entries, each entry indexed by a unique class identifier and comprising a plurality of set enable bits, a valid bit, a bypass bit, and an algorithm bit. The claim is rejected based on the same rationale as in the rejection of claims 22 and 24. Ar'507 further describes the set associative bits (Ar'507 LRU bits), different replacement algorithm bits (Ar'507: program bits). Ar'058 and Ar'507 do not describe the bypass bit. However, McClure describes a cache tag structure having a bit that when enable, the corresponding cache entry will be bypass (McClure's column 4 lines 13-35). It would have been obvious to one of ordinary skill in the art at the time of invention to include the bypass indicator as suggested by McClure in Ar'058's system thereby using the cache more effectively by allowing it to be bypassed in the situation the cache is malfunctioning (McClure's column 4 lines 16-35).

As in claim 28, the claim recites wherein the a set of the L2 cache is replaced as a function of the replacement eligibility and a replacement algorithm indicated by the algorithm bit. The claim rejected based on the same rationale as in the rejection of claim 27.

Claim 31,39 rejected based on the same rationale as in the rejection of claim 28.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 3/14/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER